Notice of Allowability	Application No.	Applicant(s)	
	09/459,305	FURUHATA, TOMOYUKI	
	Examiner	Art Unit	
	Thien F Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01/26/04*.

2. ☒ The allowed claim(s) is/are *13,15-19,30 and 32-54*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Thien Tran

THIEN TRAN
PRIMARY EXAMINER

DETAILED ACTION

Examiner's amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Alan S. Raynes on April 15, 2004.

The application has been amended as follows:

Amend the title as follows: --Semiconductor devices, circuit substrates and electronic devices--.

Claim 39, line 9, delete "field effect transistors" insert --memory cell means--.

Claim 39, line 10, delete "transistors" insert --memory cell means--.

Allowable Subject Matter

Claims 13, 15-19, 30 and 32-54 are allowed.

The following is an examiner's statement of reasons for allowance: prior art references do not teach or render obvious a semiconductor device comprising a groove in the semiconductor substrate at a position between the first and second cell areas; and a connecting area extending under the groove within the semiconductor substrate, the connecting area electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the connecting

area has an electric resistance which is lower than at least one of the sources and drains of the first and second cell areas.

Prior art references do not teach or render obvious a semiconductor device comprising the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane; a groove located in the semiconductor substrate at a position between the first and second memory cell areas; and a connecting area electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than any of the first and second source/drain regions, wherein the connecting area extends under the groove in the semiconductor substrate.

Prior art references do not teach or render obvious a semiconductor device comprising a connecting area electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, and wherein an impurity concentration of the connecting area is higher than impurity concentrations of the first source/drain regions and higher than impurity concentrations of the second source/drain regions; and a groove in the semiconductor substrate above at least a portion of the connecting area, wherein no portion of the first and second floating gates is positioned within the groove.

Prior art references do not teach or render obvious a semiconductor device comprising the first and second field effect transistors each including a floating gate structure, wherein the floating gate structure of the first and second transistors is

positioned a distance away from the groove; and a conducting region connecting a source/drain of the first field effect transistor to a source/drain of the second filed effect transistor, the conducting region being positioned below the groove and the conducting region having a lower resistance than at least one of the source/drain regions.

Prior art references do not teach or render obvious a semiconductor device comprising a grove extending into the semiconductor substrate at a position between the first and second field effect transistors, wherein the groove has a depth and at least part of the connecting area has an impurity depth that is offset from that of the adjacent source/drain regions by the depth of the groove.

Prior art references do not teach or render obvious a semiconductor device comprising a groove extending into the semiconductor substrate at a position between the first and second memory cell means; and connecting means positioned under the groove for electrically connecting the first and second memory cell means, the connecting means having a resistance lower than that of the source/drain regions; wherein the first and second memory cell means each include a floating gate structure, wherein the floating gate structure of the first and second memory cell means is positioned a distance away from the groove.

Prior art references do not teach or render obvious a semiconductor device comprising sources and drains formed in the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate; a groove in the semiconductor substrate at a position between the first and second cell areas; and an impurity area extending under the groove within the semiconductor

substrate, the impurity area electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the impurity area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas.

Prior art references do not teach or render obvious a semiconductor device comprising the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane; a groove located in the semiconductor substrate at a position between the first and second memory cell areas; an impurity area electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the impurity area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, wherein the impurity area extends under the groove in the semiconductor substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 15, 2004

Thien Tran

THIEN TRAN
PRIMARY EXAMINER